IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	**Mail Stop: Missing Parts**
Hiroyuki KANDA et al.	:	Docket No. 2004_0586A
Serial No. 10/824,344	:	**Confirmation No. 6329**
Filed April 15, 2004	:	
PLATING METHOD		

TRANSLATOR'S DECLARATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

I, Ryoji Kosugi, declare and say:

that I am thoroughly conversant in both the Japanese and English languages;

that I am presently engaged as a translator in these languages;

that the attached document represents a true English translation of the above-identified Japanese application entitled "PLATING METHOD".

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signed this 13th day of August, 2004.

Ryoji Kosugi

Translator Ryoji Kosugi

PLATING METHOD

BACKGROUND OF THE INVENTION

Field of the Invention:

The present invention relates to a plating method of filling fine recesses formed in a substrate such as a semiconductor wafer or the like with a metal to form an interconnect circuit, and more particularly to a plating method of plating a substrate with a plated film with high adhesion without producing voids in the plated film even when relatively narrow recesses and relatively broad recesses are co-present in the substrate.

Description of the Related Art:

In recent years, copper has widely been used as an interconnect material for use in semiconductor devices. One general process for forming interconnects of copper is a damascene process in which fine recesses such as via holes, trenches, etc. are formed in an insulating film formed on a substrate, and then an interconnect metal such as copper or the like is deposited on the insulating film, after which any extra interconnect metal is removed by CMP or the like.

According to the damascene process, before an interconnect metal such as copper or the like is deposited, a barrier layer such as of TaN, Ta, or the like for preventing copper atoms from being diffused into an insulating film is formed on the surfaces of the substrate and the recesses. Then, if copper is to be deposited by performing electroplating, a seed layer serving as a current supply layer for electroplating is formed on the barrier

layer on the surfaces of the substrate and the recesses. The seed layer is generally formed by PVD or CVD. PVD is widely used as it can form a seed layer capable of high adhesion to the barrier layer.

Heretofore, the following problems have arisen in forming a seed layer on a surface of a recess: If a recess has a broad width and a small aspect ratio, then a seed layer can uniformly be formed uninterruptedly on the entire surface of the recess. However, if a seed layer is formed by anisotropic PVD on a surface of a recess that has a narrow width and a large aspect ratio, then an amount of the seed layer material deposited on the sidewall of the recess is reduced, and the seed layer formed on the sidewall of the recess is made thin. If the width of the recess is narrower and the aspect ratio is larger, then the seed layer deposited at the opening of the recess overhangs the opening, reducing the area of the opening.

Even when an attempt is made to embed metal (plated film) in a recess having such a seed layer by electroplating, the opening of the recess is closed by the metal before the metal is embedded in the recess, leaving voids in the metal embedded in the recess.

It is conceivable that the film thickness of the seed layer may be reduced in order to achieve the enough area of the opening of the recess. If the film thickness of the seed layer is reduced, however, the film thickness of the seed layer formed on the sidewall of the recess is further reduced, eventually causing other problems in that the seed layer is discontinued and includes a portion whose resistance is extremely large. If

electroplating is performed onto the surface of a substrate having a recess covered with such a discontinuous seed layer, no plated film is deposited on the discontinuous region of the seed layer, tending to form voids, which are in contact with the sidewall of the recess, within the metal that is embedded in the recess.

For the above reasons, it is necessary to perform electroplating of good adhesion on a substrate, which has a recess having a large aspect ratio, while avoiding both the generation of voids caused within metal by the closure of the opening of the recess and the generation of voids caused within metal by the discontinuity of a seed layer.

There has been disclosed a technique for solving the above problems by reinforcing an incomplete ultra-thin seed layer formed in a recess with a metal (plated film) formed by performing conformal plating using a plating solution containing complex copper ions, thus producing a current supply layer, and then performing electroplating to embed a metal in the recess (see USP No. 6,197,181 and Japanese laid-open patent publication No. H6-349952).

Similarly, there has also been disclosed a technique for reinforcing a seed layer with a metal (plated film) that is formed by performing electroless plating (see Japanese laid-open patent publication No. H7-193214, USP No. 5,913,147, and IEEE 2001, pages 30 through 32, pages 33 through 34, and pages 277 through 279).

However, even when a seed layer is reinforced by a metal (plated film) formed by performing conformal plating, if the

adhesion of the reinforced metal to the barrier layer is insufficient, then the problem of a migration that occurs from use cannot be said as being solved though an interconnect appears to be formed entirely in the recess immediately after the plating. This is the reason why the above techniques have not been practical in the field of semiconductor fabrication.

A process of plating copper or the like directly on a barrier layer without using a seed layer has also been developed. However, there is a limitation on barrier layer materials that are used, and the process is not sufficiently reliable.

Recently, there are available substrates in which relatively narrow recesses and relatively broad recesses are co-present. There has been a demand for embedding a metal free of voids therein with increased adhesion to a barrier layer, in a recess having a narrow width and a large aspect ratio in such a substrate.

The present invention has been made in view of the above drawbacks. It is an object of the present invention to provide a plating method of plating a substrate with a plated film of a metal such as copper or the like with high adhesion to a seed layer without producing voids in the plated film at a high throughput, not only in recesses having a broad width and a small aspect ratio, but also in recesses having a narrow width and a large aspect ratio, even if relatively narrow recesses and relatively broad recesses are co-present in the substrate.

SUMMARY OF THE INVENTION

According to the present invention, a substrate having a

relatively narrow recess and a relatively broad recess defined in a surface thereof is prepared, first plating is performed under plating conditions for filling a metal in the narrow recess, and then second plating is performed under plating conditions for filling a metal in the broad recess.

With the recent advance in PVD technology and technological developments such as atomic layer deposition, it is becoming possible to form a complete seed layer even in recesses having a narrow width and a high aspect ratio. According to the present invention, on the premise that a complete seed layer has been formed, plating conditions suitable for embedding a metal in narrow recesses and plating conditions suitable for embedding a metal in broad recesses are appropriately changed to form a void-free plated metal film with high adhesion to the seed layer in the recesses.

For example, plating under plating conditions for a relatively high bottom-up capability is suitable for embedding a metal in narrow recesses, and plating under plating conditions for a relatively high leveling capability is suitable for embedding a metal in broad recesses.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional view schematically showing an impregnation plating apparatus which is preferably used in a plating method according to the present invention;

FIGS. 2A through 2C are diagrams showing different current recipes upon plating;

FIGS. 3A through 3D are cross-sectional views of different

plated films after first plating in Example 1; and

FIGS. 4A through 4C are cross-sectional views of different plated films after second plating in Example 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A substrate such as a semiconductor wafer or the like to be plated by a plating method according to the present invention has a mixture of relatively narrow recesses and relatively broad recesses in its surface. The narrow recesses in the substrate have a width, for example, less than 0.2 μm. The aspect ratio (AR) of the recesses having such a width is often 4 or more. On the other hand, the relatively broad recesses have a width, for example, of 0.2 μm or more and an aspect ratio which is generally less than 4.

For plating the above substrate by the plating method according to the present invention, a barrier layer such as of TaN, Ta, or the like is formed on the entire surface (to be plated) of a substrate having recesses defined therein according to a common procedure, and then a seed layer is formed according to PVD, CVD, or the like. For the formation of a seed layer, PVD is preferably used because it can form a seed layer capable of high adhesion to the barrier layer. Particularly, because of its excellent ability to form a seed layer on a sidewall of a recess, it is preferable to use a process such as self-ionized sputtering (SIS) or self-ionized plasma sputtering (SPS).

The substrate with the seed layer formed on its surface is then subjected to the plating method according to the present invention. The plating method according to the present

invention is basically performed by first plating under such plating conditions as to fill a metal (plated film) in relatively narrow recesses and, subsequently, second plating under such plating conditions as to selectively fill a metal (plated film) in relatively broad recesses. The plating conditions for carrying out the second plating may be changed in a certain range.

The first plating is performed under plating conditions for a relatively high bottom-up capability, and the second plating is performed under plating conditions for a relatively high leveling capability. The term "relatively" is used here for the reason that the first plating exhibits a certain leveling capability and the second plating exhibits a certain bottom-up capability, and a comparison between these plating indicates that the bottom-up capability is higher in the first plating than in the second plating, and the leveling capability is higher in the second plating than in the first plating.

Several methods are available for performing the first plating with the high bottom-up capability and the second plating with the high leveling capability. Examples of those methods are as follows:

(1) A method of changing the cathode current density (hereinafter referred to as "current density") upon plating thereby to change plating conditions of the first plating and the second plating.

(2) A method of changing additives of a plating solution used upon plating thereby to change plating conditions of the first plating and the second plating.

(3) A method of changing plating solution compositions used

upon plating thereby to change plating conditions of the first plating and the second plating.

(4) A method of changing relative speeds of a plating area and a plating solution upon plating thereby to change plating conditions of the first plating and the second plating.

According to the above-described method (1), the current density at the time of the first plating is made lower than the current density at the time of the second plating. In this case, it is preferable to use a plating solution containing an additive of a high bottom-up capability as plating solutions for use in the first plating and the second plating. Reducing the current density during the second plating is able to cause the additive to exhibit its bottom-up capability more effectively. It is determined by experimentation or the like how much the current density is to be lowered to increase the bottom-up capability. If a standard copper sulfate plating solution is used, for example, then the current density upon the first plating, which requires the bottom-up capability, is generally in the range from 0.1 to 1.5 A/dm^2, and the current density upon the second plating, which requires the leveling capability, is generally in the range from 2 to 7 A/cm^2. It is thus possible to make the current density upon the second plating greater than the current density upon the first plating for thereby increasing the leveling capability and making the plating rate upon the second plating higher than the plating rate upon the first plating to perform a time-consuming process of filling a metal in broad recesses in a short period of time.

After a metal is filled in relatively narrow recesses by

performing the first plating, a reverse electric field may be applied for a short period of time, as shown in FIG. 2A, to etch an overplated film on the surfaces of the narrow recesses, thus removing the additive in the overplated film. The period of time for applying the reverse electric field is generally in the range from 1 to 10 seconds, and preferably from 1 to 4 seconds.

In FIG. 2A, the current density during the first plating and the current density during the second plating are varied discontinuously. For example, as shown in FIG. 2B, the first plating and the second plating may be performed by varying the current density so as to increase gradually. Alternatively, as shown in FIG. 2C, the first plating and the second plating may be performed by varying the current density so as to increase linearly.

According to the above-described method (2), a plating solution containing an additive of a relatively high bottom-up capability is used as the plating solution during the first plating, and a plating solution containing an additive of a relatively high leveling capability is used as the plating solution during the second plating. For example, since a copper sulfate plating solution generally contains as additives a suppressor (precipitation suppressor: for conformal), an accelerator (increasing the bottom-up capability), and a leveler. An additive including more of a component called an accelerator is used in the plating solution for the first plating, and an additive including more of a component called a leveler is used in the plating solution for the second plating.

Components serving as the suppressor, components serving

as the accelerator, and components serving as the lever are well known. Representative examples of them are given as follows: Polypropylene glycol, polyethylene glycol, their polymers, high-molecular surfactant such as ethylene oxide, etc. are suppressor components. Sulfur-based organic compounds such as dithiobis-alkane-sulfonic acids, such as 4,4-dithiobisbutane sulfonic acid, 3,3-dithiobispropane sulfonic acid, etc. or their salts are accelerator components. Organic dye compounds such as safranine, thioflavine, Dye 300, Cy5, etc. are leveler components. This method may be carried out using two plating solutions containing different additives, or may be carried out by adding a leveler component, for example, when changing from the first plating to the second plating.

Whether a plating solution including more of a component called an accelerator is used as the plating solution for the first plating or not is reflected by the concentration of sulfur in the plated film. For example, if copper sulfate plating is carried out using a plating solution including more of an accelerator, then it is common for sulfur atoms to have a density of 1×10^{18} atoms/cm^3 or more at a depth of 0.5 μm in a plated copper film having a thickness of 1 μm. If a plating solution not including more of an accelerator is used, on the other hand, then the density of sulfur atoms at a depth of 0.5 μm in a plated copper film under the same conditions does not reach 1×10^{18} atoms/cm^3 or more.

According to the above-described method (3), furthermore, a plating solution having a high metal ion concentration and a high anion concentration is used as the plating solution during

the first plating, and a plating solution having a low metal ion concentration and a low anion concentration is used as the plating solution during the second plating. For example, a copper sulfate plating solution contains copper ions as metal ions and sulfuric acid ions as anion ions. If a plating solution with high concentrations of these ions is used, then the bottom-up capability is increased, and if a plating solution with low concentrations of these ions is used, then the leveling capability is increased. For carrying out this method, a first plating solution having a high metal ion concentration and a high anion concentration and a second plating solution having a low metal ion concentration and a low anion concentration may be prepared, and these plating solutions may be used.

According to the final method (4), the bottom-up capability and the leveling capability are adjusted based on a change in the relative speeds of a plating area and a plating solution upon plating. In spin plating, for example, the relative speed of the plating solution is determined by the rotational speed of the substrate and the speed of the plating solution jet. If the rotational speed of the substrate (the speed in the horizontal direction with respect to the substrate) is high, the bottom-up capability is increased, and the leveling capability is lowered. If the speed of the plating solution jet (the speed in the vertical direction with respect to the substrate) is high, the bottom-up capability is lowered, and the leveling capability is increased. Therefore, the bottom-up capability and the leveling capability can be adjusted by using these properties.

With the method according to the present invention, the

above methods may be used singly or in combination for achieving more appropriate bottom-up and leveling capabilities.

If an acid plating solution is used, then it is preferable to carry out the following method when the substrate is brought into the plating solution: Specifically, an oxide film may be formed in contact with air on the surface of a seed layer formed on the surface of a substrate, and the oxide film may be dissolved in contact with an acid plating solution. In this case, the surface of the seed layer is etched by the acid plating solution, and the thin seed layer may be eliminated in extreme cases, exposing the barrier layer.

Before the substrate is brought into contact with the plating solution, a plating voltage is applied between the substrate and the anode held in contact with the plating solution for starting to reduce the oxide film on the surface of the seed layer or deposit a plated film from the time when the substrate is brought into contact with the plating solution. This method is generally referred to as hot entry.

In the hot entry, when the substrate is brought into contact with the plating solution, a portion of the substrate first contacts the plating solution, and then the area of contact between the plating solution and the substrate increases progressively until the entire surface to be plated of the substrate contacts the plating solution. As the area of contact between the plating solution and the substrate changes, the electric resistance of the system changes greatly. In the hot entry, therefore, it is often customary to perform a voltage control process for controlling the voltage applied between the

substrate and the anode at a predetermined value. If the hot entry is performed under current control, then it is necessary to apply a voltage limiter to ensure that no voltage higher than a preset value will be applied between the substrate and the anode.

If a large voltage is set in the hot entry, then film thickness irregularities of the plated film occur between the portion of the substrate which is initially brought into contact with the plating solution and the portion of the substrate which is finally brought into contact with the plating solution. Therefore, until the substrate is brought into full contact with the plating solution, it is preferable to use as small a voltage as possible for preventing the seed layer from being dissolved.

After the hot entry is finished, if plating under the initial conditions is to be continued, the voltage control may switch to the current control, but may remain in action. Particularly, if the seed layer is thin, an initial large sheet resistance changes to a reduced resistance due to the deposition of a plated metal film on the seed layer, making it possible to supply an appropriate current that matches the resistance of the seed layer. It is of course possible to use the voltage control in the first plating and the second plating. If the current density is changed in the first plating and the second plating, the voltage may be correspondingly changed in the voltage control thereby to perform the first plating with a low current density and the second plating with a high current density, as with the current control.

The method according to the present invention as described

above can be carried out using a conventional plating apparatus for semiconductor substrates. A more preferable method is an impregnation plating method using an impregnation plating apparatus shown in FIG. 1.

FIG. 1 is a cross-sectional view schematically showing an electrode head and a substrate holder of an impregnation plating apparatus. The impregnation plating apparatus has a swing arm 26, a substrate holder 36, a cathode 88, and a seal member 90. The impregnation plating apparatus has a ball bearing 92, a housing 94 having an inward protrusion 94a and a plating solution discharge port 94b, a spacer 96, an anode 98, a hollow plating solution chamber 100, and a plating solution supply pipe 102. The impregnation plating apparatus also has a plating solution introduction pipe 104 having a plating solution introduction port 104a, a plating solution discharge pipe 106, a high-resistance structure 110 having a flange 110a, narrow pipes 112, a plating power source 114, a holder 124, a vertical displacement motor 132, and a ball screw 134. The impregnation plating apparatus holds a substrate W detachably.

The electrode head of the impregnation plating apparatus has the housing 94 coupled to the free end of the swing arm 26 by the ball bearing 92, and the high-resistance structure 110 disposed in closing relation to a lower end opening of the housing 94. The inward protrusion 94a which projects inwardly is formed at a lower portion of the housing 94, and the flange 110a is formed at an upper portion of the high-resistance structure 110. The flange 110a engages the inward protrusion 94a which, with a spacer 96 interposed between the housing 94 and the high-resistance

structure 110, holding the high-resistance structure 110 in the housing 94. In this manner, the hollow plating solution chamber 10 is defined in the housing 94.

The high-resistance structure 110 is made of porous ceramics such as alumina, SiC, mullite, zirconia, titania, cordierite, or the like, or a hard porous material such as a sintered material of polypropylene or polyethylene, or a composite material thereof, or a woven or a non-woven fabric. For example, alumina-based ceramics having a pore diameter ranging from 30 to 200 μm, SiC having a pore diameter of 30 μm or less, a porosity ranging from 20 to 95 %, and a thickness ranging from 1 to 20 mm, preferably from 5 to 20 mm, or more preferably from 8 to 15 mm, is used. In this embodiment, the high-resistance structure 110 is in the form of a porous ceramics plate of alumina having a porosity of 30 % and an average pore diameter of 100 μm. When the high-resistance structure 110 is impregnated with a plating solution, though the porous ceramics plate itself is an insulating material, it causes the plating solution to enter therein in a complex pattern and follow a considerably long path in the transverse direction thereof, providing an electric conductivity smaller than that of the plating solution.

The high-resistance structure 110 is disposed in the plating solution chamber 100 and produces a high resistance to reduce the effect of the resistance of the seed layer to a negligible degree, thus reducing an in-plane difference between current densities due to the electric resistance of the surface of the substrate W for increased in-plane uniformity of the plated

film.

The anode 98 is disposed in the plating solution chamber 100 and mounted on the lower surface of the plating solution introduction pipe 104 disposed above the anode 98. The plating solution introduction port 104a of the plating solution introduction pipe 104 is connected to the plating solution supply pipe 102 which extends from a plating solution supply equipment (not shown). The plating solution discharge port 94b on the upper surface of the housing 94 is connected to the plating solution discharge pipe 106 which communicates with the plating solution chamber 100.

The plating solution introduction pipe 104 is of a manifold structure for supplying a plating solution uniformly to the surface to be plated. Specifically, the narrow pipes 112 communicating with the interior of the plating solution introduction pipe 104 are connected thereto at longitudinally spaced positions. The anode 98 and the high-resistance structure 110 have small holes defined therein in alignment with the narrow pipes 112. The narrow pipes 112 extend through those small holes and reach the lower surface of the high-resistance structure 110 or a region near the lower surface thereof.

The plating solution introduced from the plating solution supply pipe 102 into the plating solution introduction pipe 104 passes through the narrow pipes 112 to a lower portion of the high-resistance structure 110, passes through the high-resistance structure 110, fills the plating solution chamber 100, causing the anode 98 to be immersed in the plating solution. The plating solution can be discharged from the

plating solution discharge pipe 106 by evacuating the plating solution discharge pipe 106.

The anode 98 used in the above impregnation plating apparatus is made of copper (phosphorus-containing copper) containing 0.03 to 0.05 % of phosphorus in order to prevent a slime from being produced. However, the anode 98 may be made of an insoluble material.

The cathode 88 is electrically connected to the positive terminal of the plating power source 114, and the anode is electrically connected to the negative terminal of the plating power source 114. The plating power source 114 is arranged so as to be able to change the direction of the flowing current as desired.

The ball bearing 92 is suspended from the swing arm 26 via the holder 124. The sing arm 26 is vertically movable by the vertical displacement motor 132, which comprises a servomotor, and the ball screw 134. This vertical displacement mechanism may be a pneumatic actuator.

During electroplating, the electrode head is lowered until the gap between the substrate W held by the substrate holder 36 and the high-resistance structure 110 becomes 0.1 to 3 mm, for example. Then, the plating solution supply pipe 102 supplies the plating solution (plating solution) to impregnate the high-resistance structure 110 with the plating solution and fills the interior of the plating solution chamber 100 with the plating solution from the upper surface (to be plated) of the substrate W. In this manner, the surface to be plated of the substrate W is plated.

The present invention will be described in detail below with respect to examples. However, the present invention is not limited to these examples.

In the examples, a plating solution including 150 to 250 g/l of pentahydrate of copper sulfate, 20 to 100 g/l of sulfuric acid, 20 to 90 mg/l of chlorine in terms of a basic composition was used. Additives that were used include 0.05 to 20 mg/l of PEG (polyethylene glycol) having a molecular weight of 20,000 as a high-molecular surfactant for suppressing an electrodeposition reaction, 1 to 20 mg/l of 3,3-dithiobispropane sulfonic acid sodium as a sulfur-based saturated organic compound for accelerating the electrodeposition speed, and 1 to 20 mg/l of safranine as an organic dye compound for controlling the leveling of copper plating.

Example 1:

In Example 1, the first plating and the second plating were carried out by changing current densities during plating.

(1) First, a preliminary experiment in which the concentration of the sulfur-based organic compound and the concentration of the organic dye compound were changed was conducted to confirm whether voids were produced in a metal (plated film) embedded by plating in fine interconnect pattern recesses or not. The height of humps of the plated film formed by plating was also confirmed. A pattern wafer used in the experiment had a via pattern having a diameter of 0.16 μm and a depth of 0.8 μm and a via pattern having a diameter of 0.3 μm and a depth of 0.8 μm, etching in a thermal oxide film. On the wafer, there was formed a barrier layer of TaN to a thickness

ranging from 10 to 40 nm and a seed layer to a thickness ranging from 60 to 150 nm by an SIS process. The current passed during plating was in the range from 0.1 A/dm^2 to 3 A/dm^2. The cross section of the wafer after it was plated was confirmed with SEM for voids in the metal.

Table 1 below shows the experimental results. With the pattern having the diameter of 0.16 μm, the metal in the via pattern was void-free only if the concentration of the sulfur-based organic compound was high and the concentration of the organic dye compound was low. With the plating solution containing 20 mg/l of the sulfur-based organic compound and 5 mg/l of the organic dye compound, no voids were observed in the metal at a current value of in the range from 0.1 A/dm^2 to 1.5 A/dm^2, bottom voids were observed in the metal at a current value of 0.1 A/dm^2 or less, and top voids were observed in the metal column at a current value in excess of 1.5 A/dm^2. At current values in the range from 0.1 A/dm^2 to 1.5 A/dm^2, the bottom-up capability was fine, and pinch-off was suppressed. This means that the bottom-up capability depends on the concentration ratio of both of additives and there is an appropriate current condition. No voids were produced in the metal for the pattern having the diameter of 0.3 μm.

Table 1

Amount of organic dye compound (mg/l)	Amount of sulfur-based organic compound (mg/l)			
		5	10	20
	5	x/O	O/O	O/O
	10	x/O	x/O	O/O
	20	x/O	x/O	x/O

Diameter 0.16 μm/diameter 0.3 μm

O: void-free, x: voids produced

(2) Then, a pattern wafer in which a trench pattern of L/S (line and space: trench width/trench interval) = 0.18 μm/0.18 μm and L/S = 0.3 μm/0.3 μm were etched in a thermal oxide film having a film thickness of 1.0 μm and a barrier layer and a seed layer were formed thereon was used, and the height of humps produced on a plated film deposited by plating was confirmed. The current passed upon plating was 1.0 A/dm^2, the plating time was 280 seconds, and the film was plated to a thickness corresponding to 1 μm in terms of a solid film. Table 2 shows the results. It is understood from Table 2 that the height of humps is small if the concentration of the sulfur-based organic compound is low and the concentration of the organic dye compound is high.

Table 2

Amount of organic dye compound (mg/l)	Amount of sulfur-based organic compound (mg/l)			
		5	10	20
	5	30/10	80/30	120/50
	10	20/0	60/20	100/40
	20	10/0	30/10	70/20

LS: 0.18 μm/LS: 0.3 μm

The proportion of the height of humps (= b/a × 100 %), see a, b for FIG. 4A.

(3) Based on the preliminary experiments (1), (2), a plating experiment was conducted on an actual pattern wafer, using a cup-type plating apparatus for 200 mm wafers. A pattern wafer has a mixture of fine patterns having a width of 0.2 μm or less and patterns having a greater width. A depth of the pattern was in a range from 0.2 to 1.0 μm. On the pattern wafer, there was formed a barrier layer of TaN to a thickness ranging from 10 to 40 nm and a seed layer to a thickness ranging from 60 to 150 nm by an SIS process.

The plating solution that was used had a high sulfur-based organic compound concentration of 20 mg/l and a low organic dye compound concentration of 5 mg/l. The plating solution flowed at a rate ranging from 5 to 25 l/min., the plating temperature was in the range from 20 to 30°C, and the wafer was rotated at a rotational speed in the range from 10 to 250 rpm. Current conditions are such that according to the plating current recipe shown in FIG. 2A, the first plating was performed in the first step to embed a void-free metal in fine interconnect patterns and the second plating was performed in the second step under conditions for a high throughput and conditions for a better in-plane uniformity of the plated film.

Specifically, in the first plating, the wafer was plated for 25 to 50 seconds with an initial current value corresponding to 1.0 A/dm^2. At 2.0 A/dm^2, a reverse electric field was applied for 0.5 to 5 seconds to remove the additive from the surface. Thereafter, in the second plating, patterns other than the fine

interconnects were plated at a current value ranging from 2 to 7 A/dm^2 to form a plated film until its film thickness finally reached 1 μm.

FIGS. 3A through 3D schematically show cross sections of plated films after the first plating. FIG. 3A shows a metal (plated film) 4a embedded in a fine recess 2a having a width of 2 μm or less, for example, formed in the surface of a substrate, according to the first plating under the condition of the current density of 0.1 A/dm^2 or less. In this case, since the seed layer of the fine recess 2a is thin, a current is less liable to flow, and the plated film 4a is less likely to be precipitated. In addition, because the seed layer is etched, a bottom void 6 or a side void is easily produced in the plated film 4a. FIG. 3C shows a metal (plated film) 4a embedded in a fine recess 2a having a width of 2 μm or less, for example, according to the first plating under the condition of the current density of 1.5 A/dm^2 or less. In this case, it can be seen that the pinch-off rate is higher than the bottom-up rate, making it easy to form a top void 8 in the plated film 4a. On the other hand, FIG. 3B shows a metal (plated film) 4a embedded in a fine recess 2a having a width of 2 μm or less, for example, according to the first plating under the condition of the current density ranging from 0.1 A/dm^2 to 1.5 A/dm^2. In this case, it can be seen that no bottom voids and no top voids are produced in the plated film 4a. FIG. 3D shows a metal (plated film) 4a embedded in a broad recess 2b having a width of 2 μm or more, for example, formed in the surface of a substrate. In this case, it can be seen that a plated film 6a is formed in a nearly conformal state due to the influence

of the suppressor.

FIGS. 4A through 4C schematically show plated films after the second plating. FIGS. 4A through 4C illustrate that the height of humps on the plated film formed by the second plating changes depending on the width of the recess. Specifically, FIG. 4A shows a state in which a metal (plated film) 4a is embedded in a fine recess 2a having a width of 2 μm or less, for example, according to the first plating and thereafter a plated film 4b is formed according to the second plating. In this case, the height of a hump (= b/a × 100 %) of the plated film 4b formed according to the second plating process is large. With a slightly wider recess 2c, as shown in FIG. 4B, the height of a hump of the plated film 4b formed according to the second plating is smaller. With a wider recess 2b, as shown in FIG. 4C, a concave plated film 4b is formed by the second plating.

As described above, the first plating and the second plating are performed under different two-step current conditions for embedding fine patterns and forming a plated film with good in-plane film thickness uniformity at a high throughput.

Example 2:

In Example 2, the first plating and the second plating were carried out by changing additive components during plating.

Plating was performed using two cells having plating solutions containing different sulfur-based organic compound and organic dye compound concentrations with a cup-type plating apparatus for 200 mm wafers. In the first plating, a plating solution having a high sulfur-based organic compound

concentration of 20 mg/l and a low organic dye compound concentration of 5 mg/l was used, and the wafer was plated for 25 to 50 seconds with a current value corresponding to 1.0 A/dm^2 under the conditions of Example 1, thus embedding a metal (plated film) in a fine interconnect pattern.

In the second plating, a plating solution having a low sulfur-based organic compound concentration of 5 mg/l and a high organic dye compound concentration of 10 mg/l was used, and a metal (plated film) was embedded in patterns other than fine interconnect patterns at a current density ranging from 2 to 5 A/dm^2, finally achieving a plated film thickness of 1 μm. By performing the first plating and the second plating under two-step current conditions, fine patterns can be embedded. By performing the second plating using a plating solution having different additive concentrations, highly smooth plated film was realized.

The method according to the present invention as described above can plate a substrate under plating conditions suitable for embedding both narrow recesses and broad recesses.

Therefore, it is possible to form a void-free, high-adhesion plated film of metal such as copper or the like in recesses, thus fabricating a stable-performance semiconductor substrate.